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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P8517 Total Pages 3

First Named Inventor or Application Identifier Opher Kahn

Express Mail Label No. EL143554720US

ADDRESS TO: **Assistant Commissioner for Patents**
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Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 19+cover sheet)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 3)

4. X Oath or Declaration (Total Pages 5)(unsigned)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. X Other: Express Mail Certification and Attorney Signature page.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _____

18. **Correspondence Address**
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Serial/Patent No.: * * * * Filing/Issue Date: Herewith
Client: Intel Corporation
Title: A METHOD AND APPARATUS FOR RESUMING OPERATIONS FROM A LOW LATENCY WAKE-UP LOW POWER STATE
BSTZ File No.: 042390.P8517 Atty/Secty Initials: EHT/JSD/rap
Date Mailed: 2/14/00 Docket Due Date: * * * *

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- ☐ Application - Rule 1.53(b) CIP (_____ pgs.)
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- ■ Declaration & POA (5 pgs.) (unsigned)
- ☐ Disclosure Docs & Orig & Copy of Inventor's Signed Letter (_____ pgs)
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- ■ Information Disclosure Statement & PTO-1449 (3 pgs.)
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- ☐ Reply Brief (_____ pgs.)
- ☐ Response to Notice of Missing Parts
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UNITED STATES UTILITY PATENT APPLICATION

FOR

A METHOD AND APPARATUS FOR RESUMING OPERATIONS FROM A LOW LATENCY WAKE-UP LOW POWER STATE

Inventors:

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42390.P8517

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A METHOD AND APPARATUS FOR RESUMING OPERATIONS FROM A LOW LATENCY WAKE-UP LOW POWER STATE

BACKGROUND

1. Field

The present disclosure pertains to the field of power management for a processing system and particularly to resuming operations upon exiting a low power state.

2. Description of Related Art

Power management is an increasingly important feature in systems such as computer systems. However, users are generally less interested in power conservation features that significantly impact the response time and performance of their systems. Thus, implementing low power states with low latency resumption is desirable.

The Advanced Configuration and Power Interface (ACPI) Specification 1.0b (Revision 1.0b of this open industry specification is available at http://www.teleport.com/~acpi/) provides a uniform set of definitions, power management states, and the like for implementing power conservation features in a computing system. The ACPI Specification defines the S1 power state as a low latency power state in which all system context is maintained (see § 9.1.1).

A typical system arrangement asserts the STPCLK# pin and waits for the processor to enter the stop grant state. At this point, the system may or may not shut down clocks to

the processor and/or to external buses or other circuitry. Prior art systems place system memory into a self-refresh or a suspend-refresh state. Refresh is maintained by the memory itself or through some other reference clock that is not stopped during the sleeping (S1) state.

One example of a memory architecture is the Rambus™ memory architecture available from Rambus Corporation of Mountain View, California. Some Rambus™ parts offer various power conservation modes (see "Direct Rambus™ Memory for Mobile PCs" also available from Rambus Corporation). Active, nap, standby, and PwrDown (powerdown) modes are available. A Rambus™ Dynamic Random Access Memory (RDRAM) automatically transitions to standby mode at the end of a transaction. When a memory transaction request is sent out to the memory array, the appropriate RDRAM device exits standby and services the request.

Power consumption may be further reduced by placing RDRAMs in a nap mode or a powerdown mode. Nap and powerdown modes may be entered by sending commands to the memory. From both the nap mode and the powerdown mode, a resynchronization time is required by the RDRAM for memory system's delay locked loop to synchronize the RDRAM interface to the channel clock.

Unfortunately, these memory power conservation states do not directly map into power conservation states enumerated by the ACPI Specification. The system designer is left to determine which states to use at what time, and how to enter and exit such states. Particularly puzzling is how to perform re-initialization in such a memory architecture when exiting low latency states such as the ACPI S1 state where nap or powerdown memory power conservation modes are likely to be used.

When exiting nap and powerdown states, the memory requires clock re-initialization. Exiting the ACPI S1 state, however, typically results in returning directly to operating system code (in the memory subsystem) after deassertion of the STPCLK# interrupt. Accordingly, it may not be possible to execute low level software such as BIOS software in response to a transitions out of the S1 state. Consequently, the memory subsystem may not be sufficiently re-initialized to allow memory accesses to commence.

Brief Description of the Figures

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings.

Figure 1 illustrates one embodiment of a system utilizing presently disclosed techniques.

Figure 2 is a flow diagram for operations of one embodiment of the system of Figure 1.

Figure 3 illustrates additional details of initialization operations performed by one embodiment.

Detailed Description

The following description provides a method and apparatus for resuming operations from a low latency wake-up low power state. In the following description, numerous specific details such as memory types, signal names and logic partitioning/integration choices are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be practiced without such specific details. In other instances, control structures and gate level circuits have not been shown in detail in order not to obscure the invention. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate logic circuits without undue experimentation.

Some embodiments advantageously allow initialization sequences to be performed in conjunction with exiting low latency low power states. This initialization may be important to ensure proper operation of memory subsystems that have complex initialization requirements. Some embodiments perform such initialization using hardware to avoid any reliance on the memory subsystem as the memory subsystem may not yet be operational. Likewise, some embodiments perform the initialization operations in a manner transparent to the operating system and/or to the central processor.

Figure 1 illustrates one embodiment of a system utilizing presently disclosed techniques. The system of Figure 1 includes a memory interface 110 and a hub interface 102 which are coupled to a processor 140 and a graphics engine 150. As indicated by a

dashed box 120, the processor 140, the memory interface 110, the hub interface 102 and the graphics engine 150 may be integrated into a single component. Also within the component is a clock and power unit 106 which may control global clocking a power supply for the memory interface 110 , the processor 140, and the graphics engine 150. The memory interface 110 is also coupled to a memory subsystem 160. The memory subsystem 160, when the system is operational, contains an operating system 170. The hub interface 102 is coupled to an I/O control hub (ICH) 180. The ICH 180 is coupled to generate a stop clock signal (STPCLK#) on a signal line 186 for the processor 140. The ICH 180 is also coupled to a secondary bus 185 which has coupled thereto a memory device 190 storing BIOS routines.

The embodiment of Figure 1 utilizes logic in both the ICH 180 and the memory interface 110 to exit from a low latency low power state and to appropriately initialize a memory subsystem 160 so that execution may be resumed. Accordingly, the memory subsystem 160, the operating system 170 and the processor 140 need not be involved.

The operation of one embodiment of the system illustrated in Figure 1 is illustrated in the flow diagram of Figure 2. In block 200, low power state entry conditions are detected. Detecting conditions such as inactivity or low battery power which warrant the entry into a low power state may be performed by hardware, software, or combination of both. Known or otherwise available techniques may be used to do so. Additionally, a user request such as a shutdown command, a special power button, a hot key, or keyboard or lid closure may trigger low power state entry. Once it is determined that a low power state should be entered, the system also typically selects which of a set of low power states to enter. For example, the ACPI specification describes low power

system states S1-S5. In this case, a low latency, low power state such as the ACPI S1 state is selected. A low latency, low power state maintains system context and allows a relatively rapid resumption of system execution. As such, complete re-initialization of components such as the memory subsystem 160 may not be feasible or desirable in a low latency, low power state.

Next, in block 205, memory control logic 135 places the memory subsystem 160 in a self-refresh mode. Since complete re-initialization may not be performed upon resumption from the low latency, low power state, the hardware maintains at least some of the configuration information determined at boot time as indicated in block 210. To maintain this information (typically stored in registers within the memory interface 110), power is maintained to the memory interface during the low latency, low power state. Additionally, as indicated in block 212, a bit may be set indicating which low power mode is being entered. The BIOS may indicate the power state by writing a value stored in the memory interface 110. In other embodiments, such a value may be set using other software or hardware techniques and may be located elsewhere, such as in the ICH 180. Additionally, the bit may be set in a different order with respect to other low power state entry operations so long as the bit is set before the low power state is actually entered.

The global clock and power unit 106 shuts down clocks in an appropriate order to prevent malfunctions. For example, global S1 state logic 108 may control gating of the clock to the CPU and/or the memory interface or other components. Glitches or other malfunctions may be avoided by gating clocks to, for example, the memory interface when a phase locked loop for the component is shut down. Additionally, prior to entry into the low power state, S1 messaging logic 184 may generate a message for the memory

interface 110 to indicate that the memory interface 110 should flush any write buffers. This may alternatively be performed in conjunction with placing he memory in a self-refresh state (block 205), and may be sequenced differently in different embodiments. The memory interface 110 may then return a message via messaging logic 125 to the ICH 180 to indicate these operations are complete and that actual entry into the low latency low power state may now occur.

As indicated in block 215, the low latency, low power state is then entered. Again, the ACPI S1 state is one example of an appropriate low latency, low power state. The system remains in the low latency, low power state until a wake-up event occurs as indicated in block 220. At this point, S1 exit detect logic 182 detects the low power state exit event which occurs as indicated in block 225. In response, S1 messaging logic 184 sends a message (e.g., S1 exit) via a bus 181 (e.g., a hub link bus) to the memory interface 110 as indicated in block 227.

S1 messaging logic 125 in the hub interface 102 receives and decodes the hub link S1 state exit message from the ICH 180 and responsively enables memory resume logic 130. The memory resume logic 130 sequences through a series of initialization commands to reinitialize the memory subsystem 160 as indicated in block 230. The memory control logic 135 may have a predefined set of instructions that it typically receives from software such as the BIOS. The memory resume logic 130 may sequence through an internally generated series of such commands in order to perform the proper initialization operations. Therefore, the memory resume logic 130 may emulate a software routine that initializes the memory control logic 135. The routine emulated may be a subset of the BIOS routine used at boot when the memory is first initialized or when

another low power state is exited (e.g., the ACPI S3 state).

Since the memory resume logic 130 itself sequences through the series of initialization commands, interaction is not required from the processor 140 or the memory subsystem 160. Advantageously, this transparency allows complex initializations to be performed at a time when the memory subsystem is unavailable. Moreover, since states such as ACPI S1 typically resume directly to the operating system 170 (which is stored in the memory subsystem 160), this transparency may be required as there may be no other opportunity for the processor 140 to execute a code sequence prior to needing to access the memory subsystem 160.

For example, in a system which utilizes a Rambus™ memory subsystem, putting the memory subsystem in a nap state or a powerdown state requires that certain initialization operations be performed prior to the memory subsystem resuming normal operations and returning any data from memory. Thus, if a system enters the ACPI S1 state and expects to exit by executing operating system code, the memory subsystem 160 will be unavailable to retrieve that operating system code. Thus, the intervention of hardware memory resume logic 130 may allow the ACPI S1 state to be used in a system with a Rambus™ memory subsystem.

Details of the initialization operations performed in block 230 for one embodiment are shown in the flow diagram of Figure 3. In block 300, the memory interface control logic is initialized by the memory resume logic 130. In the embodiment of Figure 1, the memory interface control logic is the memory control logic 135. In embodiments utilizing a Rambus™ memory subsystem, the memory control logic 135 may be a Rambus ASIC Cell (RAC) which may be initialized according to Rambus

specifications (e.g., execute a RAC initialization operation and set control register values as needed). These operations are performed well after the appropriate clocks are running and stable. In block 310, the memory resume logic 130 sends a clock synchronization command and the system waits for memory subsystem clocks to synchronize. For example, the system may wait for the Direct Rambus Clock Generator (DRCG) to lock to the Clock To Memory (CTM) clock.

As indicated in block 320, the memory resume logic 130 sends a command to set a current control register to a predetermined value. For example, the current control register may be set to a midpoint value. A midpoint value may be appropriate since a low power state is being exited and complete re-calibration may be needed..The midpoint value advantageously limits the maximum number of adjustments that may need be made (maximum of one-half the total range in either up or down directions). As indicated in block 330, memory core initialization operations may then be performed. These may include a series of pre-charge and refresh operations as needed to restore the memory subsystem to normal operation.

Returning to Figure 2, the memory interface 110 sends a message to the ICH 180 after the sequence of initialization operations has been completed as indicated in block 232. This message indicates that the memory interface has completed initialization operations and is prepared to resume normal operations. Accordingly, the ICH 180 deasserts the stop clock signal on the signal line 186 to the processor 140 as indicated in block 234. Then, as indicated in block 240, normal operation resumes, and the operating system or other software can resume execution of code stored in the memory subsystem 160.

Thus, a method and apparatus for resuming operations from a low latency wake-up low power state is disclosed. While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art upon studying this disclosure.

What is claimed is:

1. An apparatus comprising:

a processor;

an operating system to control a plurality of power management states, one of said power management states being a low latency low power state;

a memory subsystem that requires initialization commands to exit a memory low power state;

control logic to detect exiting of said low latency low power state and to responsively generate a plurality of initialization commands to remove said memory subsystem from said memory low power state prior to allowing execution of the processor to resume.

2. The apparatus of claim 1 wherein said low latency low power state is a state from which the apparatus resumes without executing BIOS routines.

3. The apparatus of claim 1 wherein the low latency low power state is an ACPI S1 state and wherein said memory low power state is one of a nap state and a powerdown state.

4. The apparatus of claim 1 wherein said control logic comprises:

low power state exit detection logic;

memory resume sequencing logic.

5. The apparatus of claim 4 wherein said memory resume sequencing logic is to receive an indication of exiting the low latency low power state from the low power state exit detection logic and is to allow deassertion of a stop clock signal after said plurality of initialization commands have been executed by the memory resume sequencing logic.

6. The apparatus of claim 5 wherein said memory resume sequencing logic is included in a memory interface and said low power state exit detection logic is included in an I/O control hub (ICH), said apparatus further comprising:

first messaging logic to transmit a low power state exit message to said memory interface;

second messaging logic to transmit an end of low power state exit message back to said ICH after said memory interface completes said plurality of initialization commands in response to said low power state exit message.

7. The apparatus of claim 1 wherein said plurality of initialization commands comprises:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

8. The apparatus of claim 7 wherein setting the current control register comprises setting the current control register to a midpoint value.

9. The apparatus of claim 7 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

10. An apparatus comprising:

messaging logic coupled to receive a low power state exit message;

memory system resume logic coupled to receive said low power state exit message from said messaging logic, said memory system resume logic to sequence through a plurality of initialization commands prior to generating a signal to cause a processor to exit a low power state.

11. The apparatus of claim 10 wherein said messaging logic is further to return an end of low power state exit message subsequent to completion of said plurality of initialization commands by said memory system resume logic.

12. The apparatus of claim 11 further comprising:

low power state exit detection logic to detect an exiting condition for one of a plurality of a low power states and to generate the low power state exit message.

13. The apparatus of claim 12 wherein the signal is a deassertion of a stop clock signal which is generated in response to said end of low power state exit message.

14. The apparatus of claim 13 wherein said low power state is an ACPI S1 state.

15. The apparatus of claim 10 wherein said plurality of initialization commands comprise:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

16. The apparatus of claim 15 wherein setting the current control register comprises setting the current control register to a midpoint value.

17. The apparatus of claim 15 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

18. A method comprising:

detecting an event to cause an exit from a low latency low power state;

initializing a memory subsystem transparently to an operating system;

exiting the low latency low power state.

19. The method of claim 18 wherein initializing comprises:

initializing memory interface control logic;

waiting for a clock circuit to lock;

setting a current control register;

performing memory core initialization operations.

20. The method of claim 19 wherein setting the current control register comprises setting the current control register to a midpoint value.

21. The method of claim 19 wherein performing memory core initialization operations comprises performing a sequence of pre-charge and refresh operations.

22. The method of claim 18 wherein detecting comprises:

reading a bit set by BIOS upon entry into said low latency low power state;

sending a resume message from an I/O control hub to memory interface logic.

23. The method of claim 22, after initializing, further comprising:

returning a initialization complete message to the I/O control hub;

deasserting a stop clock signal.

24. The method of claim 18 wherein exiting the low latency low power state comprises deasserting a stop clock signal to a processor.

25. The method of claim 18 further comprising:

detecting a low power state entry condition;

setting a bit to indicate to indicate the low latency low power state is selected

from a plurality of low power states.

Abstract

A method and apparatus for resuming operations from a low latency wake-up low power state. One embodiment provides a system including a processor, an operating system, and a memory subsystem that requires initialization commands to exit a memory low power state. Control logic detects exit from an operating system low latency low power state and responsively generates a plurality of initialization commands to remove the memory subsystem from the memory low power state prior to deasserting a stop clock signal and allowing execution to resume.

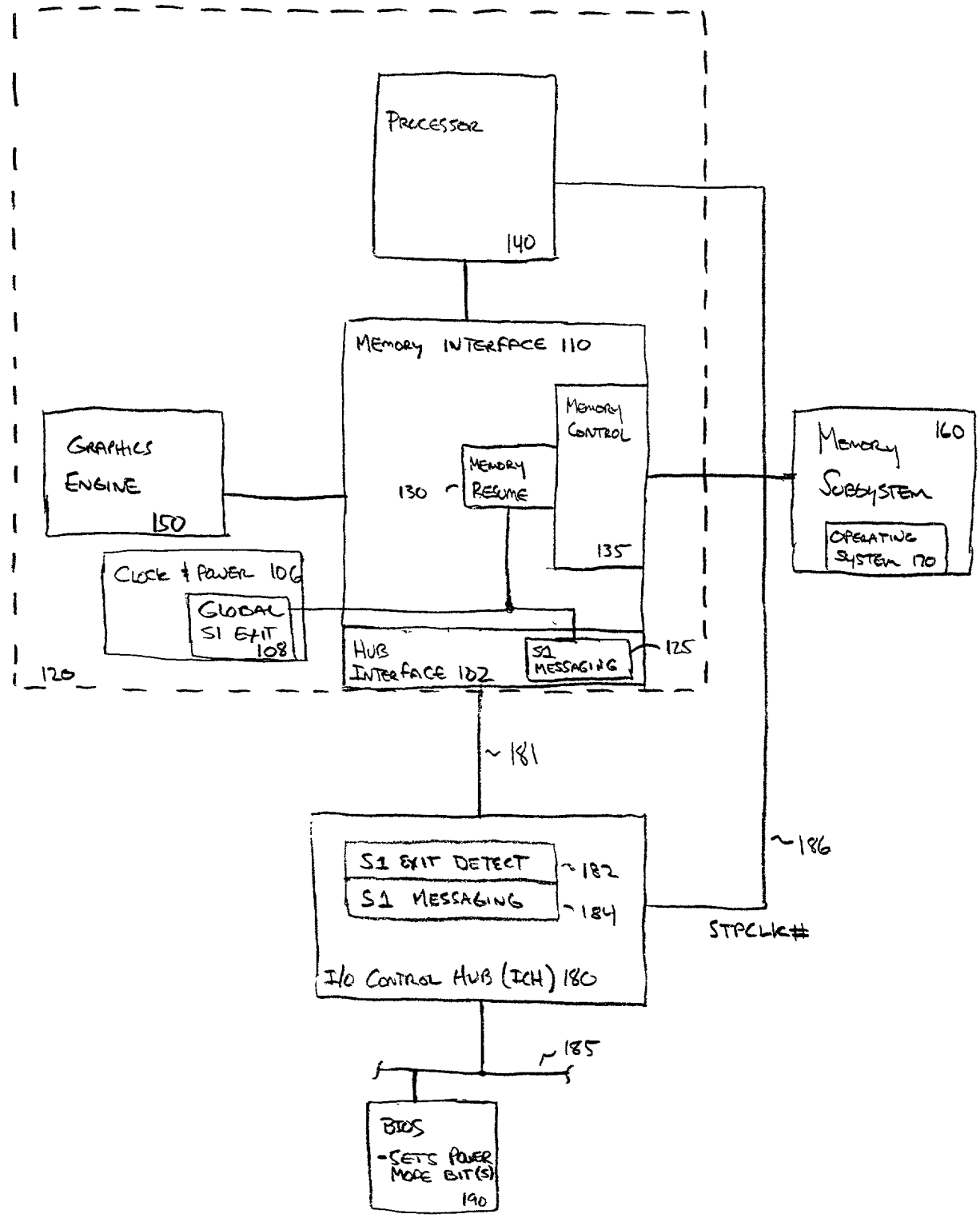

FIG. 1

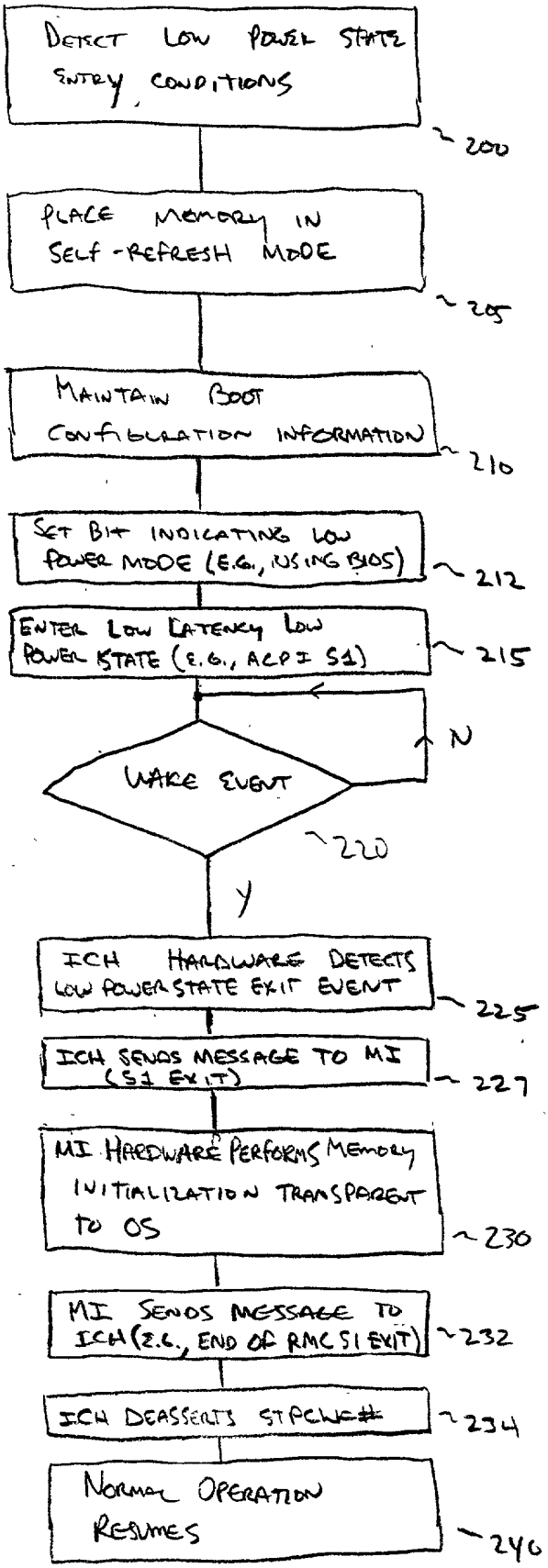

FIG. 2

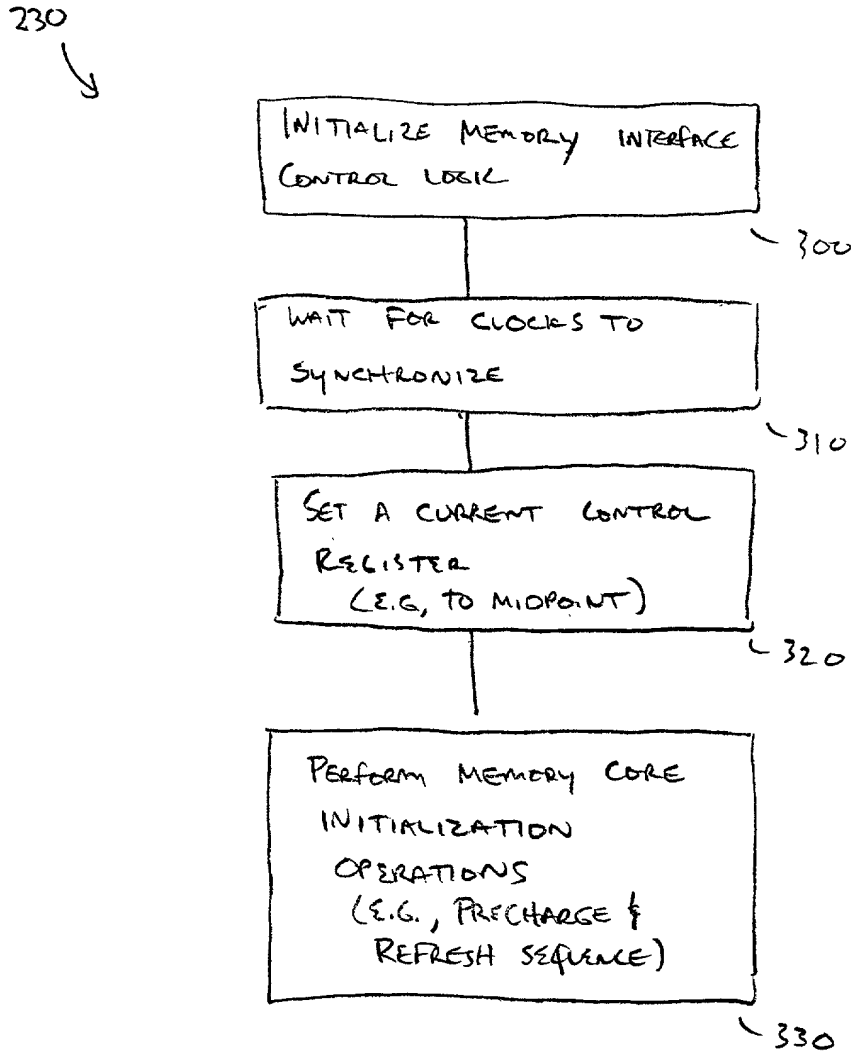

FIG. 3

Attorney's Docket No.: 042390.P8517 PATENT

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(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
A METHOD AND APPARATUS FOR RESUMING OPERATIONS FROM A LOW LATENCY WAKE-UP LOW POWER STATE

the specification of which

XX is attached hereto.
___ was filed on _____ as
United States Application Number _____
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and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Jeffrey S. Draeger **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** Jeffrey S. Draeger **(Name of Attorney or Agent)**, **(408) 720-8598.**

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Inventor's Signature _____ Date _____

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Full Name of Third/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

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APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.